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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: **PAU ET AL.**	
Serial No. **09/712,509**	
Confirmation No. **9109**	Examiner: **A. RAO**
Filing Date: **November 14, 2000**	Art Unit: **2613**
For: **METHOD OF VARYING THE BIT RATE OF THE DATA STREAM OF CODED VIDEO PICTURES**	

APPELLANT'S APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief together with the requisite $340.00 large entity fee for filing a brief. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. **01-0484.**

(1) Real Party in Interest

The real party in interest for the present application is the assignee, STMicroelectronics S.r.l.

(2) Related Appeals and Interferences

At present there are no related appeals or interferences.

(3) Status of the Claims

Claims 10-36 are pending in the application, all of which are being appealed herein.

(4) Status of the Amendments

All amendments have been entered and there are no further pending amendments. A copy of the claims involved in this appeal is attached hereto as Appendix A.

(5) Summary of the Claimed Subject Matter

As discussed on page 6, lines 14-34 in the background section of the application, sequences of video broadcasting are transmitted or are recorded on a variety of channels and supports or media, each with their own capacity, speed and cost. Distribution of a film for example, starting from a master recording, may be made on a DVD or via satellite or cable. The available transmission band may be different from the one allocated during the coding phase of the video sequence.

This raises a problem of re-adapting, to the characteristics of new media, a bitstream belonging to video pictures originally coded for a channel with a different bit-rate. Using an MPEG2 system as an example, an MPEG2 decoder and MPEG2 encoder are connected together, as best shown in FIG. 1 from the application and reproduced below for convenience, for producing an output bitstream of coded digital video data having a desired bit-rate (B2 Mbit/s) different from a bit-rate (B1 Mbit/s) of an input bitstream of coded digital video data. The tasks necessary to perform this function are listed on page 7, lines 14-18 for the MPEG2 decoder and lines 24-33 for the MPEG2 encoder. This results in a transcoding process that has a high computational complexity.

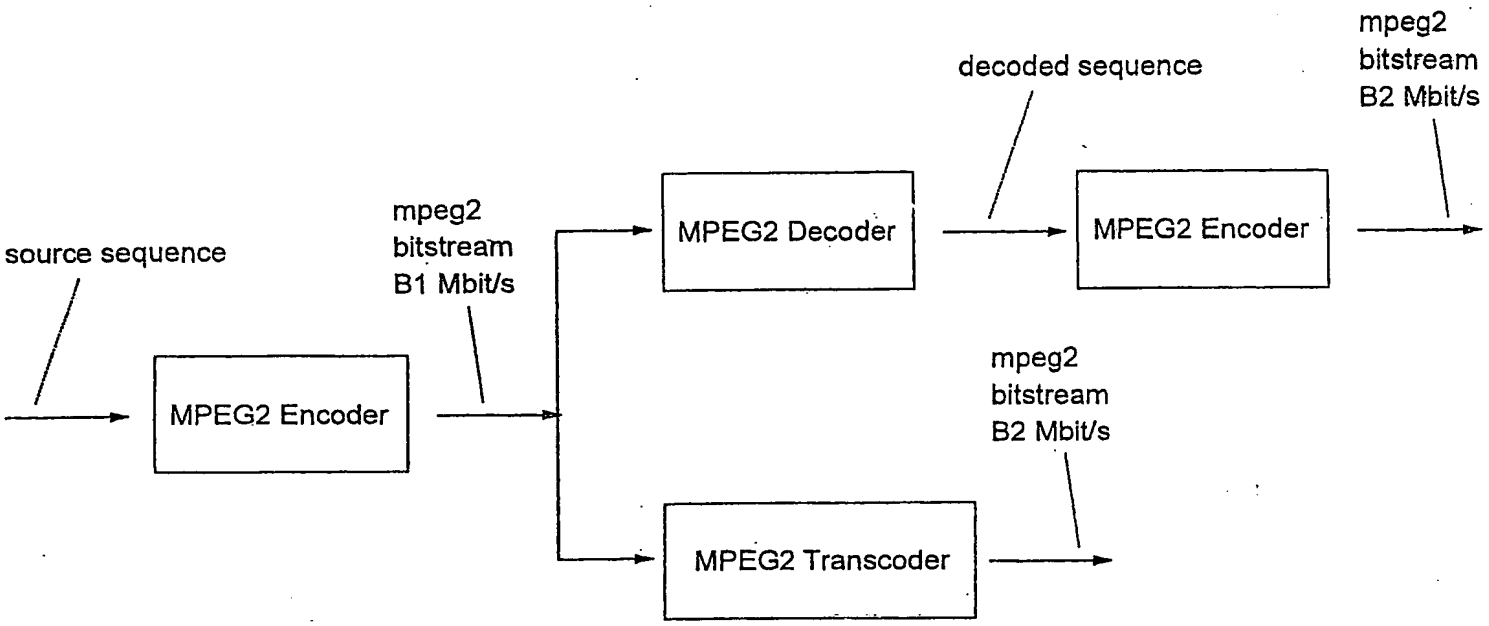

FIG. 1 from the Appellant's specification

Independent method Claims 10 and 17 and independent device Claims 23 and 31 advantageously change the bit-rate of a bitstream of video pictures use a reduced number of steps and simplifying the resources for doing so. In particular, an output bitstream of coded digital video data is produced having a desired bit-rate different from a bit-rate of an input bitstream of coded digital video data.

Independent method Claim 10, for example, recites dividing the input bitstream into a sequence of coded data and into a sequence of control bits, and modifying the sequence of control bits as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits, as best shown in FIG. 4a from the application and reproduced below for convenience, and as discussed on page 12, lines 12-28 in the application.

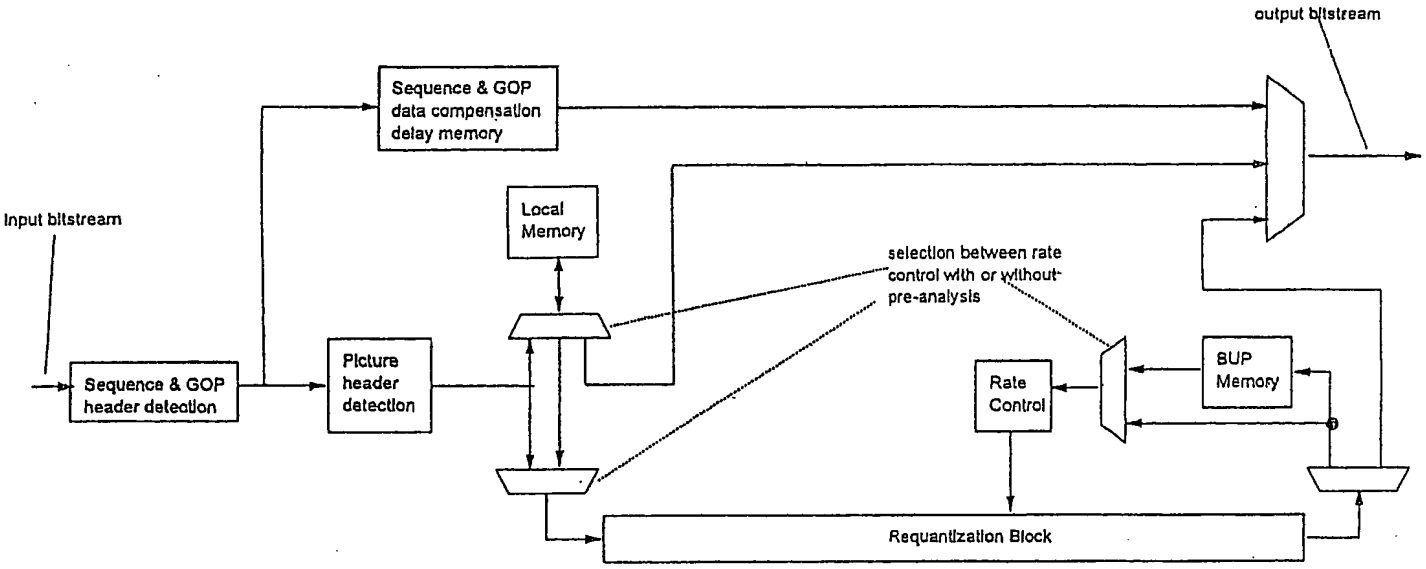

FIG. 4a from the Appellant's specification

The method further comprises decoding a sequence of coded data for producing an intermediate sequence of data, and quantizing with a pre-established step and coding the intermediate sequence of data for producing an output sequence of coded data. The output sequence of control bits and the output sequence of coded data are merged for producing the output bitstream of coded digital video data having the desired bit-rate.

The method advantageously divides the input bitstream into a sequence of coded data and into a sequence of control bits. Since the bit rate may be determined by the number of bits dedicated to the coding of the quantized DCT coefficients of the prediction error, the bit rate may be varied by operating on the quantization parameter. The portion of the bitstream that does not influence the reduction of the bit rate may be simply copied rather than processed - hence, the method comprises dividing the input bitstream into a sequence of coded data and into a sequence of control bits.

The sequence of coded data are subjected to the decoding and quantizing steps which are performed in the requantization block as best shown in FIG. 4b from the application and reproduced below for convenience, and as discussed on page 12, lines 29-35 in the application.

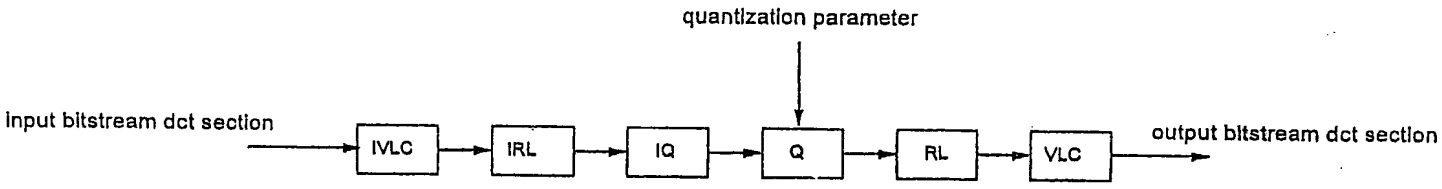

FIG. 4b from the Appellant's specification

Independent method Claim 17 is similar to independent method Claim 10 except this claim further recites that the decoding of the sequence of coded data is performed using a Huffman decoding followed by a run-length decoding for producing the intermediate sequence of data. Independent method Claim 17 further recites that quantizing and coding the intermediate sequence of data are performed using a run-length coding followed by a Huffman coding for producing the output sequence of coded data.

Independent device Claim 23 is similar to independent method Claim 10 and recites a first circuit (sequence & GOP header detection block in FIG. 4a) for separating the input bitstream into a sequence of coded data and into a sequence of control bits. A second circuit (sequence & GOP data compensation delay memory in FIG. 4a) has an input for receiving the sequence of control bits. The second circuit generates a modified sequence of control bits as a function of the desired bit-rate of the output bitstream for providing an output sequence of control bits. A decoder

(such as the IVLC and IRL blocks in FIG. 4b) has an input for receiving the sequence of coded data and an output for providing an intermediate sequence of data. A quantizer (such as the Q block in FIG. 4b) quantizes the intermediate sequence of data with a pre-established step. An encoder (such as the RL and VLC blocks in FIG. 4b) connected to an output of the quantizer provides an output sequence of coded data. A third circuit (such as the multiplexer block in FIG. 4a) merges the output sequence of control bits and the output sequence of coded data for producing the output bitstream having the desired bit-rate.

Independent device Claim 31 is similar to independent device Claim 23 except this claim further recites that the decoder comprises a Huffman decoder and a run-length decoder connected in series together followed by a run-length decoding for producing the intermediate sequence of data. Independent device Claim 31 further recites that the encoder comprises a run-length coder and a Huffman coder connected in series thereto.

(6) Grounds of Rejection to be Reviewed On Appeal

Claims 10-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kadono (U.S. Patent No. 6,590,936) in view of Adolph et al. (U.S. Patent No. 6,081,295).

(7) Argument

I. The Claims Are Patentable

The Examiner cited Kadono as disclosing a method of producing an output bitstream of coded digital video data having a desired bit-rate different from a bit-rate of an input bitstream of coded digital video data as in the claimed invention. As correctly noted by the Examiner, Kadono fails to disclose an output sequence of control bits and an output sequence of coded data being merged for producing an output

bitstream of coded digital video data having a desired bit-rate. The Examiner cited the Adolph et al. patent to supply this noted deficiency of the Kadono patent.

The Applicants respectfully submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not produced. Kadono fails to disclose dividing the input bitstream into a sequence of coded data and into a sequence of control bits, and modifying the sequence of control bits as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits. Reference is directed to FIG. 1 and to column 18, line 58 through column 19, line 6 of Kadono, which provides:

> "The decoding unit **Da1** includes, instead of the inverse quantization unit **101** of the prior art decoding unit **D1**, an inverse quantization unit **101a** which subjects the output **Vg** from the VLD (variable-length decoding) unit **100** to inverse quantization, and outputs a first quantization step **Qs1** to the encoding unit **E1**. The first quantization step **Qs1** used in the inverse quantization process is identical to the quantization step used in the quantization process for the image data (first quantization process). Further, the transcoding unit **Ea1** according to this embodiment includes, instead of the quantization unit **107** of the prior art transcoding unit **E1**, a quantization unit **151** which subjects the output Tq from the DCT unit **106** to a quantization process based on a quantization control signal **Cq** supplied from the rate control unit **113** and the first quantization step **Qs1** supplied from the inverse quantization unit **101a**." (Emphasis added.)

As best shown in FIG. 1 from the Kadono patent and reproduced below for convenience, the inverse quantization

unit **101a** generates outputs **Qs1** and **IQg**. It appears that these two outputs **Qs1, IQg** are identical. As noted above, "the first quantization step output **Qs1** used in the inverse quantization process is identical to the quantization step used in the quantization process for the image data." The Applicants submit that since outputs **Qs1** and **IQg** are identical, then the inverse quantization unit **101a** does not divide the input bitstream into a sequence of coded data and into a sequence of control bits. Instead, the inverse quantization unit **101a** simply provides the same quantization step output twice.

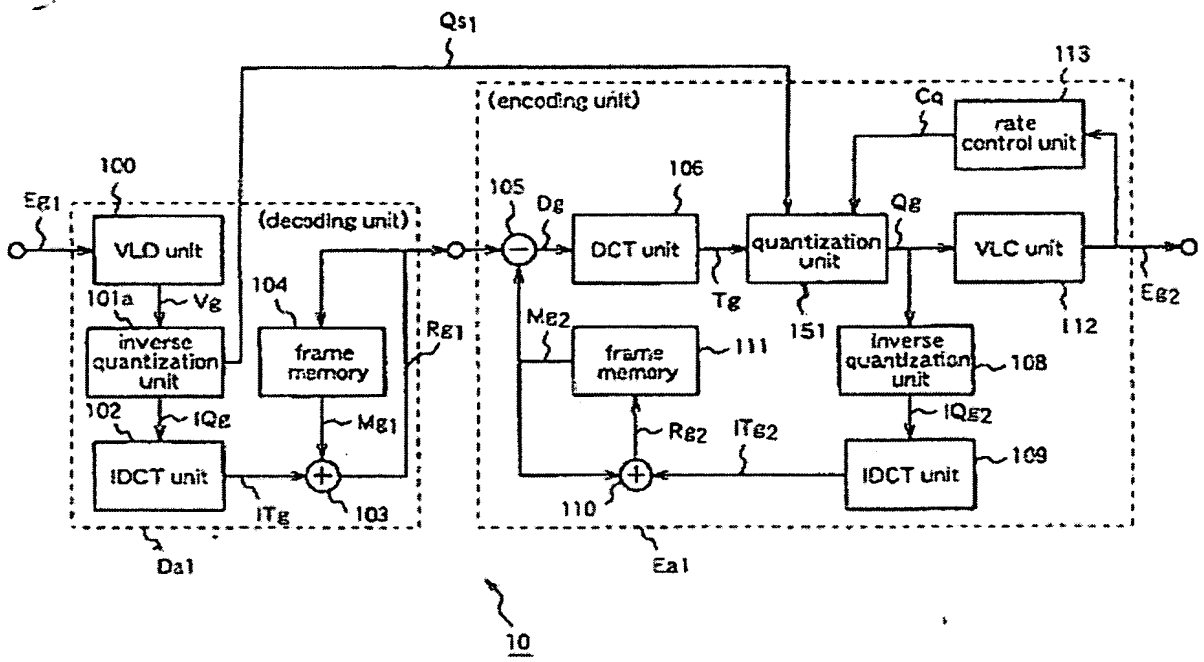

FIG. 1 of the Kadono Patent

Moreover, the first quantization step output **Qs1** is not modified as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits. Instead, the first quantization step output **Qs1** is applied as input to the quantization unit **151**. In the

quantization unit **151**, the DCT coefficients **Tg** supplied from the DCT unit **106** are subjected to a quantization process (second quantization process) on the bases of the first quantization step output **Qs1** supplied from the inverse quantization unit **101a** of the decoding unit **Da1** and the quantization control signal **Cq** supplied from the rate control unit **113**.

Referring now to FIGS. 2 and 3 of Kadono, reproduced below for convenience, the quantization unit **151** (FIG. 2) receiving the first quantization step output **Qs1** will now be discussed in greater detail. The quantization unit **151** comprises a candidate quantization step derivation unit **250**, a quantization step derivation unit **251**, and a quantizer **201**. The quantization step derivation unit **251** derives a quantization step (second quantization step) output **Qs2** in the second quantization process, on the basis of the candidate quantization step output **Qsb** and the first quantization step output **Qs1**.

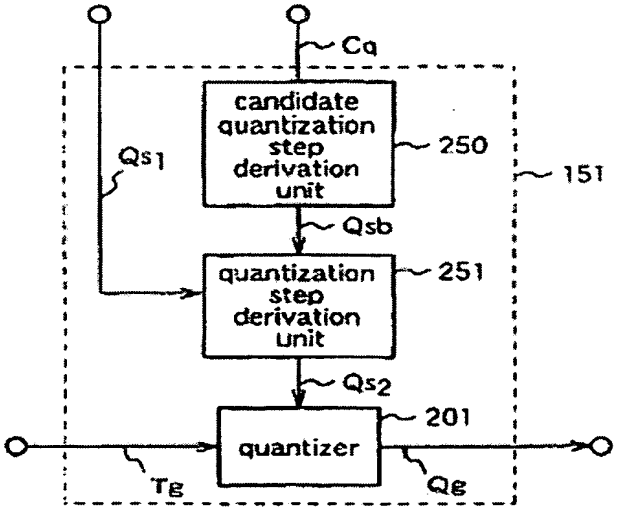

FIG. 2 of the Kadono Patent

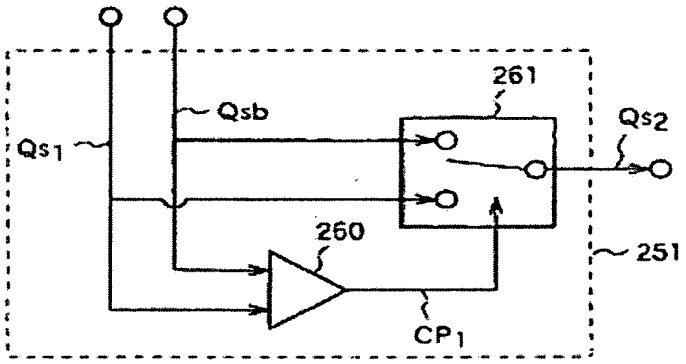

FIG. 3 of the Kadono Patent

The quantization step derivation unit **251** (FIG. 3) comprises a comparator **260** which compares the candidate quantization step output **Qsb** supplied from the candidate quantization step derivation unit **250** with the first quantization step output **Qs1** supplied from the inverse quantization unit **101a**. A switch **261** selects either the candidate quantization step output **Qsb** or the first quantization step output **Qs1** on the basis of the result of the comparison **CP1** supplied from the comparator **260**. The output from the switch **261** is output as the second quantization step output **Qs2**.

The inverse quantization unit **101a** and the quantization unit **151** process the coded data **Eg1** while suppressing an increase in the quantization error, and without increasing the number of bits. The inverse quantization unit **101a** thus performs an inverse quantization on the output **Vg** from the VLD unit **100**, and outputs the first quantization step output **Qs1**. The quantization unit **151** performs quantization with a quantization step larger than the first quantization

step output **Qs1** on the basis of the first quantization step output **Qs1** and the quantization control signal **Cq** which indicates the target number of bits of the target frame. In other words, the transcoding process for the coded data **Eg1** can be performed while suppressing an increase in the quantization error and without increasing the number of bits.

Referring now to Adolph et al., a primary bitstream **PBS** is converted into a secondary bitstream **SBS** with a different data rate, as best shown in FIG. 1 and reproduced below for convenience. The primary bitstream **PBS** is separated by a demultiplexer **DMX** into system data **SYD**, audio data **AUD** and video data **VID**. The system data **SYD** and the audio data **AUD** are each processed by a respective processor. Since Kadono fails to disclose the output sequence of control bits and the output sequence of coded data being merged for producing an output bitstream of coded digital video data having a desired bit-rate, the Examiner cited Adolph et al. to supply this noted deficiency.

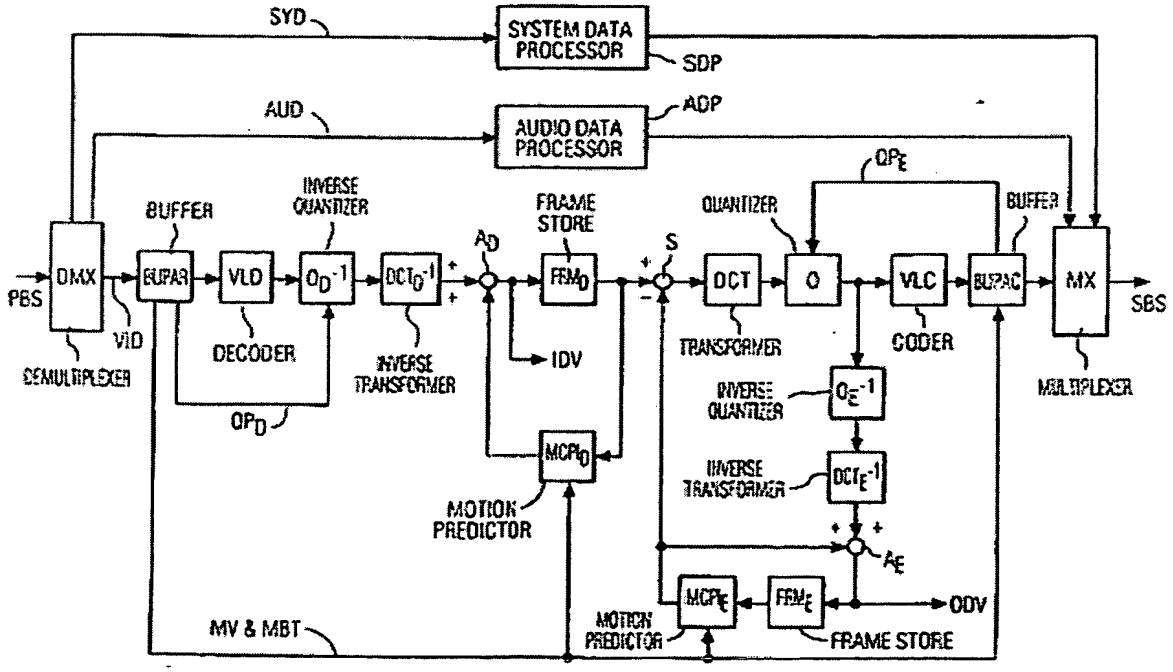

FIG. 1 of the Adolph et al. Patent

Even if Kadono discloses that the input bitstream **Eg1** has been divided into a sequence of control bits (i.e., first quantization step output **Qs1**) and into a sequence of coded data, neither Kadono or Adolph et al. discloses that the sequence of control bits is modified as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits. Instead, Kadono simply outputs **Qs1** as input to the quantization unit **151**. Adolph et al. fails to disclose that the system data processor **SDP** modifies the "control bits" (i.e., the system data **SYD**) as a function of the desired bit-rate of the secondary bitstream **SBS** as in the claimed invention.

The Applicants thus submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not produced. Accordingly, it is submitted that independent Claim 10 is patentable over Kadono in view of Adolph et al.

Independent Claims 17, 23 and 31 are similar to independent Claim 10. Therefore, it is submitted that these claims are also patentable over Kadono in view of Adolph et al. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features of the invention, are also patentable. These dependent claims require no further discussion herein.

II. Conclusion

In view of the foregoing arguments, it is submitted that all of the claims are patentable over the prior art. Accordingly, the Board of Patent Appeals and Interferences is respectfully requested to reverse the earlier unfavorable

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Serial No. **09/712,509**
Filing Date: **November 14, 2000**
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decision by the Examiner.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15th day of November, 2004.

APPENDIX A - CLAIMS ON APPEAL FOR U.S. PATENT APPLICATION SERIAL NO. 09/712,509

10. A method of producing an output bitstream of coded digital video data having a desired bit-rate different from a bit-rate of an input bitstream of coded digital video data, the method comprising:

dividing the input bitstream into a sequence of coded data and into a sequence of control bits;

modifying the sequence of control bits as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits;

decoding the sequence of coded data for producing an intermediate sequence of data;

quantizing with a pre-established step and coding the intermediate sequence of data for producing an output sequence of coded data; and

merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream of coded digital video data having the desired bit-rate.

11. A method according to Claim 10 wherein the intermediate sequence of data is dequantized before being quantized with the pre-established step.

12. A method according to Claim 10 wherein the input and output bitstreams of coded digital video data comprise MPEG data.

13. A method according to Claim 10 wherein the input and output bitstreams of coded digital video data comprise MPEG2 data.

14. A method according to Claim 10 wherein the decoding comprises performing a Huffman decoding followed by a run-length decoding; and wherein coding comprises performing a run-length coding followed by a Huffman coding.

15. A method according to Claim 10 wherein quantizing with the pre-established step comprises a feed-back rate control technique.

16. A method according to Claim 10 wherein quantizing with the pre-established step comprises a feed-back/forward hybrid rate control technique.

17. A method of producing an output bitstream of coded digital video data having a desired bit-rate different from a bit-rate of an input bitstream of coded digital video data, the method comprising:

dividing the input bitstream into a sequence of coded data and into a sequence of control bits;

modifying the sequence of control bits as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits;

decoding the sequence of coded data using a Huffman decoding followed by a run-length decoding for producing an intermediate sequence of data;

quantizing with a pre-established step and coding the intermediate sequence of data using a run-length coding followed by a Huffman coding for producing an output sequence of coded data; and

merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream of coded digital video data having the desired bit-rate.

18. A method according to Claim 17 wherein the intermediate sequence of data is dequantized before being quantized with the pre-established step.

19. A method according to Claim 17 wherein the input and output bitstreams of coded digital video data comprise MPEG data.

20. A method according to Claim 17 wherein the input and output bitstreams of coded digital video data comprise MPEG2 data.

21. A method according to Claim 17 wherein quantizing with the pre-established step comprises a feed-back rate control technique.

22. A method according to Claim 17 wherein quantizing with the pre-established step comprises a feed-back/forward hybrid rate control technique.

23. A device for producing a bitstream of coded digital video data having a bit-rate different from a bit-rate of an input bitstream of coded digital video data, the device comprising:

a first circuit for separating the input bitstream into a sequence of coded data and into a sequence of control bits;

a second circuit having an input for receiving the sequence of control bits, said second circuit for generating a modified sequence of control bits as a function of the desired bit-rate of the output bitstream for providing an output sequence of control bits;

a decoder having an input for receiving the sequence of coded data and an output for providing an intermediate

sequence of data;

a quantizer for quantizing the intermediate sequence of data with a pre-established step;

an encoder connected to an output of said quantizer for providing an output sequence of coded data; and

a third circuit for merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream having the desired bit-rate.

24. A device according to Claim 23 further comprising a dequantizer connected between said decoder and said quantizer for dequantizing the intermediate sequence of data.

25. A device according to Claim 23 wherein the input and output bitstreams of coded digital video data comprises MPEG data.

26. A device according to Claim 23 wherein the input and output bitstreams of coded digital video data comprises MPEG2 data.

27. A device according to Claim 23 wherein said decoder comprises a Huffman decoder and a run-length decoder connected in series thereto.

28. A device according to Claim 23 wherein said encoder comprises a run-length coder and a Huffman coder connected in series thereto.

29. A device according to Claim 23 further comprising a bit rate control circuit connected to said encoder for setting quantizing of the intermediate sequence of data by said quantizer.

30. A device according to Claim 23 wherein said third circuit comprises a multiplexer connected to outputs of said first circuit, said second circuit and said encoder.

31. A device for producing a bitstream of coded digital video data having a bit-rate different from a bit-rate of an input bitstream of coded digital video data, the device comprising:

a first circuit for separating the input bitstream into a sequence of coded data and into a sequence of control bits;

a second circuit having an input for receiving the sequence of control bits, said second circuit for generating a modified sequence of control bits as a function of the desired bit-rate of the output bitstream for providing an output sequence of control bits;

a decoder having an input for receiving the sequence of coded data and an output for providing an intermediate sequence of data, said decoder comprising a Huffman decoder and a run-length decoder connected in series thereto;

a quantizer for quantizing the intermediate sequence of data with a pre-established step;

an encoder connected to an output of said quantizer for providing an output sequence of coded data, said encoder comprising a run-length coder and a Huffman coder connected in series thereto; and

a third circuit for merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream having the desired bit-rate.

32. A device according to Claim 31 further comprising a dequantizer connected between said decoder and said quantizer for dequantizing the intermediate sequence of

data.

33. A device according to Claim 31 wherein the input and output bitstreams of coded digital video data comprises MPEG data.

34. A device according to Claim 31 wherein the input and output bitstreams of coded digital video data comprises MPEG2 data.

35. A device according to Claim 31 further comprising a bit rate control circuit connected to said encoder for setting quantizing of the intermediate sequence of data by said quantizer.

36. A device according to Claim 31 wherein said third circuit comprises a multiplexer connected to outputs of said first circuit, said second circuit and said encoder.